COMPUTER ARCHITECTURE QUESTIONS (OBJECTIVE TYPE)

1. _____ has been developed specifically for pipelined systems.
a) Utility software
b) Speed up utilities
c) Optimizing compilers
d) None of the mentioned
Answer: c
Explanation: The compilers which are designed to remove redundant parts of the code are called as optimizing compilers.

2. The fetch and execution cycles are interleaved with the help of _____
a) Modification in processor architecture
b) Clock
c) Special unit
d) Control unit

Answer: b
Explanation: The time cycle of the clock is adjusted to perform the interleaving.

3. Each stage in pipelining should be completed within ____ cycle.
a) 1
b) 2
c) 3
d) 4
Answer: a
Explanation: The stages in the pipelining should get completed within one cycle to increase the speed of performance.

4. To increase the speed of memory access in pipelining, we make use of _____
a) Special memory locations
b) Special purpose registers
c) Cache
d) Buffers

Answer: c
Explanation: By using the cache we can reduce the speed of memory access by a factor of 10.

5. The situation wherein the data of operands are not available is called _____
a) Data hazard
b) Stock
c) Deadlock
d) Structural hazard
Answer: a
Explanation: Data hazards are generally caused when the data is not ready on the destination side.

6. The situation wherein the data of operands are not available is called _____
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d) Structural hazard
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Explanation: Data hazards are generally caused when the data is not ready on the destination side.

7. The time lost due to the branch instruction is often referred to as _____
a) Latency
b) Delay
c) Branch penalty
d) None of the mentioned
Answer: c
Explanation: This time also retards the performance speed of the processor.

8.The algorithm followed in most of the systems to perform out of order execution is _____
a) Tomasulo algorithm
b) Score carding
c) Reader-writer algorithm
d) None of the mentioned
Answer: a
Explanation: The Tomasulo algorithm is a hardware algorithm developed in 1967 by Robert Tomasulo from IBM. It allows sequential instructions that would normally be stalled due to certain dependencies to execute non-sequentially (out-of-order execution).

9. The time interval between adjacent bits is called the_____.
a) Word-time
b) Bit-time
c) Turn around time
d) Slice time

10. Any condition that causes a processor to stall is called as _____
a) Hazard
b) Page fault
c) System error
d) None of the mentioned

11. The logic operations are implemented using _____ circuits.
a) Bridge
b) Logical
c) Combinatorial
d) Gate
Answer: c
Explanation: The combinatorial circuits means, using the basic universal gates.

12. The carry generation function: ci + 1 = yici + xici + xiyi, is implemented in _____
a) Half adders
b) Full adders
c) Ripple adders
d) Fast adders
Answer: b
Explanation: In this the carry for the next step is generated in the previous steps operation.

13. Which option is true regarding the carry in the ripple adders?
a) Are generated at the beginning only
b) Must travel through the configuration
c) Is generated at the end of each operation
d) None of the mentioned
Answer: b
Explanation: The carry must pass through the configuration of the circuit till it reaches the particular step.

14. In full adders the sum circuit is implemented using _____
a) And & or gates
b) NAND gate
c) XOR
d) XNOR
Answer: c
Explanation: sum = a ^ b ^ c (‘^’ indicates XOR operation).

15. The usual implementation of the carry circuit involves _____
a) And & or gates
b) XOR
c) NAND
d) XNOR
Answer: b
Explanation: In case of full and half adders this method is used.

16. The advantage of I/O mapped devices to memory mapped is _____
a) The former offers faster transfer of data
b) The devices connected using I/O mapping have a bigger buffer space
c) The devices have to deal with fewer address lines
d) No advantage as such
Answer: c
Explanation: Since the I/O mapped devices have a separate address space the address lines are limited by the amount of the space allocated.

17. The system is notified of a read or write operation by _____
a) Appending an extra bit of the address
b) Enabling the read or write bits of the devices
c) Raising an appropriate interrupt signal
d) Sending a special signal along the BUS
Answer: d
Explanation: It is necessary for the processor to send a signal intimating the request as either read or write.

18. To overcome the lag in the operating speeds of the I/O device and the processor we use _____
a) Buffer spaces
b) Status flags
c) Interrupt signals
d) Exceptions
Answer: b
Explanation: The processor operating is much faster than that of the I/O devices, so by using the status flags the processor need not wait till the I/O operation is done. It can continue with its work until the status flag is set.

19. The method of synchronizing the processor with the I/O device in which the device sends a signal when it is ready is
a) Exceptions
b) Signal handling
c) Interrupts
d) DMA

Answer: c
Explanation: This is a method of accessing the I/O devices which gives the complete power to the devices, enabling them to intimate the processor when they're ready for transfer.

20. The method which offers higher speeds of I/O transfers is _____
a) Interrupts
b) Memory mapping
c) Program-controlled I/O
d) DMA
Answer: d
Explanation: In DMA the I/O devices are directly allowed to interact with the memory without the intervention of the processor and the transfers take place in the form of blocks increasing the speed of operation.

21. The instruction, Add #45, R1 does _____
a) Adds the value of 45 to the address of R1 and stores 45 in that address
b) Adds 45 to the value of R1 and stores it in R1
c) Finds the memory location 45 and adds that content to that of R1
d) None of the mentioned
Answer: b
Explanation: The instruction is using immediate addressing mode hence the value is stored in the location 45 is added.

22. In the case of, Zero-address instruction method the operands are stored in _____
a) Registers
b) Accumulators
c) Push down stack
d) Cache
Answer: c
Explanation: In this case, the operands are implicitly loaded onto the ALU.

23. The addressing mode which makes use of in-direction pointers is _____
a) Indirect addressing mode
b) Index addressing mode
c) Relative addressing mode
d) Offset addressing mode
Answer: a
Explanation: In this addressing mode, the value of the register serves as another memory location and hence we use pointers to get the data.

24. The addressing mode/s, which uses the PC instead of a general purpose register is _____
a) Indexed with offset
b) Relative
c) direct
d) both Indexed with offset and direct
Answer: b
Explanation: In this, the contents of the PC are directly incremented.

25. _____ addressing mode is most suitable to change the normal sequence of execution of instructions.
a) Relative
b) Indirect
c) Index with Offset
d) Immediate
Answer: a
Explanation: The relative addressing mode is used for this since it directly updates the PC.

26. The reason for the implementation of the cache memory is _____
a) To increase the internal memory of the system
b) The difference in speeds of operation of the processor and memory
c) To reduce the memory access and cycle time
d) All of the mentioned
Answer: b
Explanation: This difference in the speeds of operation of the system caused it to be inefficient.

27. The effectiveness of the cache memory is based on the property of _____
a) Locality of reference
b) Memory localisation
c) Memory size
d) None of the mentioned
Answer: a
Explanation: This means that the cache depends on the location in the memory that is referenced often.

28. The spatial aspect of the locality of reference means _____
a) That the recently executed instruction is executed again next
b) That the recently executed won't be executed again
c) That the instruction executed will be executed at a later time
d) That the instruction in close proximity of the instruction executed will be executed in future
Answer: d
Explanation: The spatial aspect of locality of reference tells that the nearby instruction is more likely to be executed in future.

29. The correspondence between the main memory blocks and those in the cache is given by _____

a) Hash function
b) Mapping function
c) Locale function
d) Assign function
Answer: b
Explanation: The mapping function is used to map the contents of the memory to the cache.

30. The copy-back protocol is used _____
a) To copy the contents of the memory onto the cache
b) To update the contents of the memory from the cache
c) To remove the contents of the cache and push it on to the memory
d) None of the mentioned
Answer: b
Explanation: This is another way of performing the write operation, wherein the cache is updated first and then the memory.

31. The address space is 22 bits the memory is 32 bit word addressable what is the memory size

a)16MB

b)512KB

c)4MB

d)1GB

Answer: a

32. In which cycle the memory is read and the contents of memory at the address containedin the PC register are loaded into in to IR.

a)Execution Cycle

b)Memory Cycle

c)Fetch Cycle

d)Decode Cycle

Answer: c

33.The part of machine level instruction, which tells the central processor what has to be done, is

a) Operation code

b) Address

c) Locator

d) Flip-Flop

Answer: a

34. A system program that combines the separately compiled modules of a program into a form suitable for execution

a) assembler

b) linking loader

c) cross compiler

d) load and go

Answer: b

35. Which parameter of computer determines its power to do various operations on data items

a) Instruction set

b)Memory size

c) Assembly language

d)Application language

Answer: a

36. The multiplier is stored in

a) PC Register

b) Shift Register

c) Cache

d) None of the above

Answer: b

37. Which methods of representation of numbers occupies large amount of memory than others?

a)sign-magnitude

b) 1's compliment

c) 2's compliment

d) Both a and b

Answer: a

38. The register used to store the flags is called as

a) Flag register

b) Status register

c) Test register

d) log register

Answer: b

39._____is used to implement virtual memory organization.
a) Page table
b) Frame table
c) MMU
d) None of the mentioned
Answer: c
Explanation: The MMU stands for Memory Management Unit.

40. _____ method is used to establish priority by serially connecting all devices that request an interrupt.
a) Vectored-interrupting
b) Daisy chain
c) Priority
d) Polling
Answer: b
Explanation: In the Daisy chain mechanism, all the devices are connected using a single request line and they're serviced based on the interrupting device's priority.

41. A bus that connects components in a multiprocessor system is called _____.
a) control bus
b) Data bus
c) Address bus
d) System bus

42. A memory connected to the common system bus is _____by all processors.
a) **Shared**
b) Partitioned
c) Distributed
d) None of the above

43. A multiprocessor system with common shared memory is called_____.
a) loosely coupled system
b) Tightly coupled system
c) Both a and b
d) None of the above

44. A_____ system is an interconnection of two more cpu with memory and I/O equipment
a) Processor
b) Synchronization
c) **Multiprocessor**
d) None of the above

45. Which among following is volatile?
a) ROM
b) EPROM
c) DPROM
d) RAM

46. Where the result of an arithmetic and logical operation are stored ?
a) **In Accumulator**
b) In Cache Memory
c) In ROM
d) In Instruction Registry

47. Which determines the address of I/O interface?
a) Register select
b) Chip select
c) **Both of above**
d) None of above

48. An exception condition in a computer system caused by an event external to the CPU is known as?
a) Halt
b) Process
c) **Interrupt**
d) None of above
Explanation:

In my own experience I found very few questions with answer "None of above", if you do not know the answer then its always better to guess among other (If there is no negative marking) ;)

49. Whenever CPU detects an interrupt, what it do with current state?
a) Save it
b) Discard it
c) Depends system to system
d) first finish it

50. The address mapping is done, when the program is initially loaded is called?
a) Relocation
b) Dynamic relocation
c) Static relocation
d) Executable relocation

51. The unit which decodes and translates each instruction and generates the necessary enable signals for ALU and other units is called
a) ALU
b) Control unit
c) CPU
d) Logical unit

52. The performance of the cache memory is measured in terms of ?
a) Hit Ratio
b) Chat Ratio
c) Copy Ratio
d) Data Ratio

53. If CPU and I/O interface share a common bus than transfer of data between two units is known as ?
a) Asynchronous
b) Clock dependent
c) Synchronous
d) Decoder independent

54. **Which interrupt establishes a priority over the various sources to determine which request should be entertained first?**
a) Polling
b) Daisy chaining
c) Priority interrupt
d) All of above

55. Which refers the execution of various software processes concurrently?
a) IOP
b) DCP
c) Multiprocessor
d) Serial Communication

56. Which system was used extensively by early mini computers?
a) Binary number
b) Decimal number
c) Hexadecimal number
d) Octal number

57. Which operation with floating point numbers are more complicated then arithmetic operation with fixed point number?
a) Logical operation
b) Arithmetic operation
c) Both of above
d) None of above

58. ____ processor has to check continuously till device becomes ready for transferring the data?

a) DMA
b) Interrupt-initiated I/O
c) IOP
d) DCP

59. Which types of register holds a single vector containing at least two read ports and one write ports ?
a) Data system
b) Vector register
c) Database
d) Memory

60. In which of the following status flags required for data transfer are present?
a) Interface Circuit
b) Parallel Line
c) Device Circuit
d) None of Above

61. Vector architectures are operated on vectors of
a) Memory
b) Data
c) Registers
d) Graph coloring

62. Specified telling that what addressing mode will be used for accessing operand, is called
a) Address specified
b) Binary-coded decimal

c) Unpacking
d) Packed decimal

63. The ISA standard Buses are used to connect,
a) GPU and processor
b) RAM and processor
c) CD/DVD drives and Processor
d) Hard disk and Processor

64. The ascending order or a data Hierarchy is
a) bytes - bit- field - record - file - database
b) bit - bytes - record - field - file - database
c) bytes -bit - record - field - file - database
d) bit - bytes - fields - record - file - database

65. SIMD represents an organization that _____.
(a) Refers to a computer system capable of processing several programs at the same time.
(b) Represents organization of single computer containing a control unit, processor unit and a memory unit.
(**c) Includes many processing units under the supervision of a common control unit**
(d) none of the above.

66. Floating point representation is used to store
a) Boolean values
b) whole numbers
c) real integers
d) integers 67.

67. In computers, subtraction is generally carried out by
a) 9's complement
b) 10's complement
c) 1's complement
d) 2's complement

68. What characteristic of RAM memory makes it not suitable for permanent storage?
a) too slow
b) unreliable

c) it is volatile
d) too bulky

69. The circuit used to store one bit of data is known as
a) Register
b) Encoder
c) Decoder
d) Flip Flop

70. Logic gates with a set of input and outputs is arrangement of_____.
a). Computational circuit
b). Logic circuit
c) Design circuits
d). Register

71. (2FAOC) 16 is equivalent to
a) (195 084) 10
b) Both a and b
c) (001011111010 0000 1100) 2
d) None of these

72.The average time required to reach a storage location in memory and obtain its contents is called the
a**)** seek time
b) turn around time
c) access time
d) transfer time

73. The idea of cache memory is based
a) on the property of locality of reference
b on the heuristic 90-10 rule
c) on the fact that references generally tend to cluster
d) all of the above

74. Von Neumann architecture is
a) SISD
b) SIMD
c) MIMD
d) MISD

75. Cache memory acts between
a) CPU and RAM
b) RAM and ROM
c) CPU and Hard Disk
d) None of these

76. Virtual memory consists of
a) Static RAM
b) Dynamic RAM
c) Magnetic memory
d) None of these

77. In a program using subroutine call instruction, it is necessary
a) initialize program counter
b) Clear the accumulator
c) Clear the instruction register
d) Reset the microprocessor

78. A Stack-organized Computer uses instruction of
a) Indirect addressing
b) Two-addressing
c) Zero addressing
d) Index addressing

79. When CPU is executing a Program that is part of the Operating System, it is said to be in
a) Interrupt mode
b) System mode
c) Simplex mode
d) Half mode

80. An n-bit microprocessor has
a) n-bit program counter
b) n-bit address register
c) n-bit ALU
d) n-bit instruction register

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82. Cache memory works on the principle of
a) Locality of data
b) Locality of memory
c) Locality of reference
d) Locality of reference & memory

83. The main memory in a Personal Computer (PC) is made of
a) cache memory
b) static RAM
c) Dynamic Ram
d) both (A) and (B)

84. A floating point number that has a O in the MSB of mantissa is said to have
a) Overflow
b) Underflow
c) Important number
d) Undefined

85. Logic gates with a set of input and outputs is arrangement of
a) Combinational circuit
b) Logic circuit
c) Design circuits
d) Register

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b) Logic circuit
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87. A k-bit field can specify any one of
a) 3k registers
b) 2k registers
c) K2 registers
d) K3 registers

88. The time interval between adjacent bits is called the
a) Word-time
b) Bit-time
c) Turnaround time
d) Slice time

89. The load instruction is mostly used to designate a transfer from memory to a processor register known as
a) Accumulator
b) Instruction Register
c) Program counter
d) Memory address Register

90. The communication between the components in a microcomputer takes place via the address and
a) I/O bus
b) Data bus
c) Address bus
d) Control lines

91. Data input command is just the opposite of a
a) Test command
b) Control command
c) Data output
d) Data channel

92. Data input command is just the opposite of a
a) generates the address of next micro instruction to be executed
b) generates the control signals to execute a microinstruction
c) sequentially averages all microinstructions in the control memory
d) enables the efficient handling of a micro program subroutine

93. A flip-flop is a binary cell capable of storing information of
a) One bit
b) Byte
c) Zero bit
d) Eight bit

94. The operation executed on data stored in registers is called
a) Macro-operation
b) Micro-operation
c) Bit-operation
d) Byte-operation

95. Self-contained sequence of instructions that performs a given computational task is called
a) Function
b) Procedure
c) Subroutine
d) Routine

96. Microinstructions are stored in control memory groups, with each group specifying a
a) Routine
b) Subroutine
c) Vector
d) Address

97. An interface that provides a method for transferring binary information between internal storage and external devices is called
a) I/O interface
b) Input interface
c) Output interface
d) I/O bus

98. Status bit is also called
a) Binary bit
b) Flag bit
c) Signed bit
d) Unsigned bit

99. The instructions which copy information from one location to another either in the processor's internal register set or in the external main memory are called

a) Data transfer instructions

b) Program control instructions

c) Input-output instructions

d) Logical instructions

100. A device/circuit that goes through a predefined sequence of states upon the application of input pulses is called

a) register

b) flip-flop

c) transistor

d) counter